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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,363	10/02/2000	Scott B. Swaney	POU920000162US1	6279

7590 08/19/2004

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,363	SWANEY ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-18, and 20-22 have been examined.

Papers Received

2. Receipt is acknowledged of amendment and request for continued examination papers submitted, where the papers have been placed of record in the file.

3. The amendment has successfully overcome the claim objection and the objection is thus withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-7, 9-10, 12-14, 16, and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Edmondson (5,471,591).

6. In regard to claim 1, Edmondson discloses a method for holding up operands of R-unit registers for a minimum number of cycles until all prior updates have completed by comparing addresses of R-unit (because there is no specific definition of the term "R-unit" in the claim or specification nor is it a term well-known in the art, the Examiner is taking it to be the name of a unit) registers in at least one queue and interlocking valid matches of said R-unit register addresses, the method comprising:

a. receiving a plurality of R-unit register addresses associated with a millicode architecture environment, said R-unit register addresses including at least

one of a millicode general register and a millicode access register; [Note column 4, line 29, where Edmondson mentions register specifiers. One of ordinary skill in the art would recognize these specifiers to be an address of sorts because it points to a specific register. Page 1, line 22 – page 2, line 2 of Applicant's specification explain that the millicode architecture is an architecture that contains registers, which may only be directly accessed by millicode instructions. Edmondson has disclosed the use of a microcode architecture that converts macroinstructions or machine instructions to microinstructions that define the operations to be performed as shown in column 8, lines 1-11 and column 11, lines 5-23. Because the microinstructions specifically define the operations and are what is actually executed as shown above and as shown in the included dictionary definition of microcode, the microinstructions have direct access to the registers of Edmondson (including general purpose registers (column 5, lines 30-33)) and no other instructions, i.e. the macroinstructions, have such access. This function of the microcode matches the Applicant given definition of millicode and thus the terms are synonymous in the context of Edmondson. Therefore, Edmondson discloses that the register addresses are associated with millicode or microcode addresses including millicode or microcode general registers.]

b. storing said R-unit register addresses in a plurality of queues; [Note that in column 4, lines 24-25, Edmondson stores his register (source and destination) specifiers (addresses) in queues.]

c. accessing said queues; [Note in column 4, lines 40-41, that Edmondson inspects said queues. It is well known in the art that in order to inspect a queue it must be accessed.]

d. comparing said R-unit register addresses; [Note in column 5, lines 9-12, that Edmondson compares a register destination specifier to a register source specifier. It has already been shown that specifier means an address.]

e. determining matches between R-unit register addresses; [In column 5, lines 40-41, Edmonson discloses that the comparators indicate a match. It has already been shown above that the comparators compare register addresses.]

f. implementing one or more write-before-read interlocks after said determining produces a valid match, said one or more write-before-read interlocks being implemented until said comparing is no longer active, whereby operands of R-unit registers are updated during a operand prefetching period with a minimum number of cycles. [In column 5, lines 40-41 Edmondson shows that if there is a match, the current instruction is stalled. It is well known to one of ordinary skill in the art that this stall is in fact an interlock. Column 4, lines 37-42 show the case when the register operands are found to match due to a read-after-write (same as a write-before-read) conflict, causing a

read-after write stall. Column 4, lines 9-19 show that the stall is implemented until the previous instruction (the write instruction) completes execution, and thus writes to the register that will be read. Once the write instruction completes, there is no longer a write address since the write has been completed. Thus the comparing is no longer active since there is nothing to compare. Therefore, the interlock is implemented until said comparing is no longer active. The ending section of the claim that states "whereby operands of..." is known as a whereby clause. Since this section merely states the result of the previous limitations and is not necessitated by the rest of the claim, the section does not limit the scope of the claim and will not be given patentable weight. See MPEP 2106.]

7. In regard to claim 2, Edmondson discloses the method of claim 1 wherein said interlock causes a millicode read instruction not to execute (column 28, lines 43-47, where as shown previously, the stall is the interlock).

8. In regard to claim 3, Edmondson discloses the method of claim 1 wherein said plurality of queues includes a write queue (column 27, line 61, destination queue), pre-write queue (prefetch queue) and a read queue (column 27, line 60, source queue). The pre-write queue is disclosed as a prefetch queue (column 26, line 64). [This queue holds register addresses (identifiers) that are later sent to the write queue (Figure 7, elements 38 and 69; column 27, lines 42-49), hence it acts as a pre-write queue.]

9. In regard to claims 5, Edmondson discloses the method of claim 3 wherein said comparing includes comparing said R-unit register addresses sent to said read queue

against said R-unit register addresses sent to said write queue (column 5, line 9-12, destination and source specifiers).

10. In regard to claim 6, Edmondson discloses the method in claim 3 wherein said determining includes matching valid R-unit register addresses of said write queue and read queue (column 5, line 9-12, destination and source specifiers). [Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).]

11. In regard to claim 7, Edmondson discloses the method in claim 3 wherein said determining includes matching valid R-unit register addresses of said pre-write queue and read queue (column 5, line 9-12, destination and source specifiers). [The pre-write queue information acts as the destination specifier in this case as it will be written and is an input to the read queue (Figure 7, operand bus). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).]

12. In regard to claim 9, Edmondson discloses the method of claim 1 wherein said interlocks prevent millicode read instructions from being processed (column 28, lines 43-47, stalls).

13. In regard to claim 10, Edmondson discloses the method in claim 1 wherein said write queue accumulates R-unit register addresses (column 4, lines 51-52, register destination specifiers).

14. In regard to claim 12, Edmondson discloses a system for holding up R-unit operands for a minimum number of cycles until all prior updates have completed by comparing R-unit (because there is no specific definition of the term "R-unit" in the claim or specification nor is it a term well-known in the art, the Examiner is taking it to be the

name of a unit) register addresses in at least one queue and interlocking valid R-unit register address matches, the system comprising:

a. a plurality of queues for storing R-unit register addresses (Figure 7, elements 37 and 38) associated with a millicode architecture environment, said R-unit register addresses including at least one of a millicode general register and a millicode access register; [Page 1, line 22 – page 2, line 2 of Applicant's specification explain that the millicode architecture is an architecture that contains registers, which may only be directly accessed by millicode instructions. Edmondson has disclosed the use of a microcode architecture that converts macroinstructions or machine instructions to microinstructions that define the operations to be performed as shown in column 8, lines 1-11 and column 11, lines 5-23. Because the microinstructions specifically define the operations and are what is actually executed as shown above and as shown in the included dictionary definition of microcode, the microinstructions have direct access to the registers of Edmondson (including general purpose registers (column 5, lines 30-33)) and no other instructions, i.e. the macroinstructions, have such access. This function of the microcode matches the Applicant given definition of millicode and thus the terms are synonymous in the context of Edmondson. Therefore, Edmondson discloses that the register addresses are associated with millicode or microcode addresses including millicode or microcode general registers.]

b. a comparator for comparing said R-unit register addresses in said plurality of queues and determining matches between R-unit register addresses (Figure 18, element 641); and

c. a plurality of write-before-read interlocks that are implemented after valid matches of said R-unit registers are determined, said write-before-read interlocks being implemented until said comparing is no longer active, whereby operands of R-unit registers are updated during a operand prefetching period with a minimum number of cycles. [In column 5, lines 40-41 Edmondson shows that if there is a match, the current instruction is stalled. It is well known to one of ordinary skill in the art that this stall is in fact an interlock. Column 4, lines 37-42 show the case when the register operands are found to match due to a read-after-write (same as a write-before-read) conflict, causing a read-after write stall. Column 4, lines 9-19 show that the stall is implemented until the previous instruction (the write instruction) completes execution, and thus writes to the register that will be read. Once the write instruction completes, there is no longer a write address since the write has been completed. Thus the comparing is no longer active since there is nothing to compare. Therefore, the interlock is implemented until said comparing is no longer active. The ending section of the claim that states "whereby operands of..." is known as a whereby clause. Since this section merely states the result of the previous limitations and is not

necessitated by the rest of the claim, the section does not limit the scope of the claim and will not be given patentable weight. See MPEP 2106.]

15. In regard to claim 13, Edmondson discloses the system of claim 12 wherein one of said interlocks causes a millicode read instruction not to execute (column 28, lines 43-47, stalls).

16. In regard to claim 14, Edmondson discloses the system of claim 12 wherein said plurality of queues includes a write queue (Figure 7, element 38), pre-write queue (Figure 7, element 69) and a read queue (Figure 7, element 37). [The pre-write queue is disclosed as a prefetch queue (column 26, line 64). This queue holds register addresses (identifiers) that are later sent to the write queue (column 27, lines 42-49); hence it acts as a pre-write queue.]

17. In regard to claims 16, Edmondson discloses the system of claim 14 wherein said comparator compares said R-unit register addresses sent to said read queue against said R-unit register addresses sent to said write queue (Figure 18, element 641).

18. In regard to claim 20, Edmondson discloses the system of claim 13 wherein said interlocks prevent millicode read instructions from being processed (column 28, lines 43-47, stalls).

19. In regard to claim 21, Edmondson discloses the method in claim 14 wherein said R-unit addresses are accumulated in said write queue (column 4, lines 51-52, register destination specifiers).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 4, 11, 15, 17, 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edmondson in view of Hennessy.

22. In regard to claim 4:

a. Edmondson discloses the method of claim 3 as described above.

b. Edmondson's disclosure lacks the addition of a method where a bypass sends an R-unit register address when said read queue is empty.

c. Hennessy teaches that bypassing or forwarding is used to get an item early in order to avoid waiting for the item and speed up the system process (page 445, bottom paragraph). When Edmonson's read queue is empty, the incoming address is stored and then sent out right away. Placing register addresses into the read queue and removing them cost valuable cycle time. It would have been desirable to be able to avoid this added delay of the queue when it is not necessary.

d. The ability to be able to avoid any delay associated with the read queue when possible would have motivated one of ordinary skill in the art to bypass the read queue when it is empty.

It would have been obvious to one of ordinary skill in the art at the time of invention to use a method wherein a bypass sends an R-unit register address when said read queue is empty in order to avoid the delays of the read queue.

23. In regard to claim 11:

a. Edmondson discloses all the features of claim 1 as described above. Edmondson also teaches that the write queue accumulates results as shown above.

b. Edmondson does not disclose that an SRAM is used to receive the accumulated results from said write queue.

c. Hennessy teaches that SRAM is the technology of choice for registers. Edmondson's disclosed invention writes the results in the write queue to registers. Hennessy teaches that it is desirable to use faster memory closer to the processor (page 541, bottom paragraph). Registers are memory close to the processor. SRAM is the fastest standard type of memory in terms of access time as shown by Hennessy in the table on page 541.

d. The quick access time achieved by the use of SRAM technology for the registers that the write queue sends data to would have motivated one of ordinary skill in the art to use SRAM as the memory system of choice for the registers disclosed in Edmondson.

It would have been obvious to one of ordinary skill in the art at the time of invention to use SRAM technology to implement the registers disclosed by Edmondson in order to improve the access time of the registers.

24. In regard to claim 15:

a. Edmondson discloses the system of claim 14 as described above.

b. Edmondson's disclosure lacks the addition of a bypass that sends an R-unit register address when said read queue is empty.

c. Hennessy teaches that bypassing or forwarding is used to get an item early in order to avoid waiting for the item and speed up the system process (page 445, bottom paragraph). When Edmonson's read queue is empty, the incoming address is stored and then sent out right away. Placing register addresses into the read queue and removing them cost valuable cycle time. It would have been desirable to be able to avoid this added delay of the queue when it is not necessary.

d. The ability to be able to avoid any delay associated with the read queue when possible would have motivated one of ordinary skill in the art to bypass the read queue when it is empty in order to avoid the delays of the read queue.

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bypass that sends an R-unit register address when said read queue is empty in order to avoid the delays of the read queue.

25. In regard to claim 17, Edmondson discloses the system in claim 15 as described above wherein said determining includes matching valid R-unit register addresses of said write queue and read queue (column 5, line 9-12, destination and source specifiers). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

26. In regard to claim 18, Edmondson discloses the system in claim 15 wherein said comparator determines said valid R-unit register address matches between said pre-write queue and said read queue (column 5, line 9-12, destination and source specifiers). The pre-write queue information acts as the destination specifier in this case and is an input to the read queue (Figure 7, operand bus). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

27. In regard to claim 22:

a. Edmondson discloses all the features of claim 14 as described in paragraph 16 above. Edmondson also teaches that the write queue accumulates results as shown above.

b. Edmondson does not disclose that an SRAM is used to receive the accumulated results from said write queue.

c. Hennessy teaches that SRAM is the technology of choice for registers. Edmondson's disclosed invention writes the results in the write queue to registers. Hennessy teaches that it is desirable to use faster memory closer to the processor (page 541, bottom paragraph). Registers are a memory close to the processor. SRAM is the fastest standard type of memory in terms of access time as shown by Hennessy in the table on page 541.

d. The quick access time achieved by the use of SRAM technology for the registers that the write queue sends data to would have motivated one of ordinary skill in the art to use SRAM as the memory system of choice for the registers disclosed in Edmondson.

It would have been obvious to one of ordinary skill in the art at the time of invention to use SRAM technology to implement the registers disclosed by Edmondson in order to improve the access time of the registers.

Response to Arguments

28. Applicant's arguments filed July 23, 2004 have been fully considered but they are not persuasive.

29. The arguments of pages 5-7 regarding the 35 USC 102 rejections state that Edmondson does not teach or suggest a millicode architecture-based method and system for executing the functions recited in claim 1. Page 1, line 22 – page 2, line 2 of Applicant's specification explain that the millicode architecture is an architecture that contains registers, which may only be directly accessed by millicode instructions. Edmondson has disclosed the use of a microcode architecture that converts macroinstructions or machine instructions to microinstructions that define the operations to be performed as shown in column 8, lines 1-11 and column 11, lines 5-23. Because the microinstructions specifically define the operations and are what is actually executed as shown above and as shown in the included dictionary definition of microcode, the microinstructions have direct access to the registers of Edmondson (including general purpose registers (column 5, lines 30-33)) and no other instructions, i.e. the macroinstructions, have such access. This function of the microcode matches the Applicant given definition of millicode and thus the terms are synonymous in the context of Edmondson. Therefore, Edmondson discloses functions recited in claim 1 (as

described in more detail above) as being performed in a millicode architecture-based method and system.

30. Applicant also argues that Edmondson does not teach or suggest a recovery unit, or R-unit. The claim does not give indication of what an R-unit is nor is it a standard term well known in the art. In addition the specification does not disclose what an R-unit is by definition but merely describes functionality throughout the disclosure. Therefore, applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In re Self, 213 USPQ 1,5 (CCPA 1982); In re Priest, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever

enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification."In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

Therefore, the arguments regarding the R-unit are not persuasive and the examiner has interpreted the term to simply be a unit named “R”.

31. The arguments given on page 7 regarding claim 12 rely on the arguments provided for claim 1 and the same remarks given above apply to claim 12.

32. The arguments of the other pending claims have been claimed to be patentable by the Applicant due to their dependence on claims 1 and 12 though because the

arguments for these claims are not persuasive, the rejections to these claims stand as given above.

Conclusion

33. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The art cited in the previous Office Actions remain pertinent and are incorporated by reference herein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
August 12, 2004

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